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Examiner: Than Nguyen
Group Art Unit 2751

Re: Application Serial No. 08/905,356 to Belgard

Dear Examiner Nguyen:

The applicant and I were very encouraged by the fact that we were able to work out something so productively and amicably for the other application (08/905410); if at all possible, we would like to try and do the same for 08/905,356. Accordingly, I have attached a proposed amendment for you to consider for 08/905,356, in the hopes that we can work towards duplicating the earlier success, and getting these cases finally resolved.

Initially, we note that there seems to be some confusion about what kind of address translation is shown in Toy (U.S. Patent No. 4,400,774). The thrust of the Toy teachings, in fact, are only concerned with data access from a cache *subsequent* to an actual virtual-to-physical translation. There is very little detail, if any, on the actual operation of the address translation buffer.

However, there is apparently a perception at the PTO that this reference depicts a virtual-linear-physical address system, and on this basis the Examiner believes there is "inherently" a linear address generated. We think we can fairly easily demonstrate below that Toy does not generate anything resembling a linear address of the type recited in the claims, and so this should be enough to put the remaining issues to rest. If the present discussion is not enough to convince the Examiner of this fact, we welcome the opportunity to expound on the points herein in a telephone conference if need be.

First, Toy is typical of prior art systems where segmentation and paging are integrated, and hence transformation from virtual to physical addresses is performed in one step. This can be verified from the fact that the virtual address in Toy is specifically noted as having a format of the type [segment:page:word]. Toy indicates that the word address bits are not even translated. *See e.g.*, c.3 64 - 69. From this fact alone it can be seen that it is not a true separated segmentation/paging system like in the present invention, *and thus there never is any "linear" address of any kind.*

One of the objects of the present invention as disclosed in the specification on page 4 at lines 22-26, is to achieve the speed and performance advantages of *integral* segmentation and paging, and at the same time, to provide the space compaction and compatibility advantages of *separate* segmentation and paging. Integral segmentation and paging systems have a number of drawbacks, including the fact that the segments must start on page boundaries, and must be comprised of an integral number of pages, regardless of their size.